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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,291	10/02/2000	Behnam Tabrizi	1920/107	4310

2101 7590 07/12/2004

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EXAMINER	
CHU, CHRIS C	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO 90C (Rev 10/03)

Office Action Summary	Applicati n N .	Applicant(s)	
	09/677,291	TABRIZI, BEHNAM	
	Examiner	Art Unit	
	Chris C. Chu	2815	

-- The MAILING DATE of this communicati n appears on the cover sheet with the c rrespondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1, 2, 4, 7 - 18, 20 - 32, 35, 36, 40 - 45, 47 and 48* is/are pending in the application.

4a) Of the above claim(s) *23 - 31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2, 4, 7 - 18, 20 -22, 32, 35, 36, 40 - 45, 47 and 48* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on April 14, 2004 has been received and entered in the case.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 7 – 12, 14, 16 - 18, 20 - 22, 32, 35, 36, 40 – 43 and 45 are rejected under 35 U.S.C. 102(b) as being anticipated by Bates et al. (U.S. Pat. No. 5,049,978).

Regarding claims 1, 14, 16, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 6, lines 38 – 49 an electronic component comprising:

- an electronic device package (a package in Fig. 1 without cover 13) formed from an integral silicon wafer (11) having a recess (at the opening or recess in the element 11), the recess including a single (claims 1 and 16) or a first and only (claim 14) conductive region (12, at the bottom surface of the recess), the wafer and the conductive region conductively coupled so as to be at "substantially" the same electrical potential (at the point or line of the element 12 and the element 11 are connected to each other has the "substantially" same electrical potential);

- a bare die electronic device (14) having a top, a bottom, sides, and a plurality of terminals (16 and 17), including a non-top terminal (17) and a top terminal (16; claim 14), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), and wherein the non-top terminal is electrically coupled to the conductive region by the conductive bonding material (column 6, lines 38 – 49), and the top terminal (16) is electrically coupled to a second conductive region (the elements 21; claim 14); and
- a dielectric material layer (18) disposed so as to form a planar surface over the recess that is level with or higher than the top of the device such that at least a portion of the first and second conductive regions are essentially planar (claim 14).

Regarding claim 2, Bates et al. discloses in e.g., Fig. 1 and column 4, line 38 - 55 the conductive region (12, at the bottom surface of the recess) being formed by metallization.

Regarding claim 7, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 8, lines 37 – 67 a plurality of metallized bumps (21 and 22) in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal (the terminal 16 connected to the element 21 and the terminal 17 connected to the element 22) .

Regarding claim 8, Bates et al. discloses in e.g., Fig. 1 the package including a top (at the top surface of the element 18) and a bottom (at the bottom surface of the elements 11 and 12); and the bumps are located above the top of the package.

Regarding claim 9, Bates et al. discloses in e.g., Fig. 1 the device (14) being a vertical device and the bottom of the device is coupled to the package in the recess.

Regarding claim 10, Bates et al. discloses in e.g., Fig. 1 a second conductive region (the element 21 and the circuits that are connected the elements 16 and 21) coupled to a terminal (16) other than the non-top terminal (17).

Regarding claim 11, Bates et al. discloses in e.g., Fig. 1 a plurality of contact (21 and 22) including at least a first contact (22) and a second contact (21), the first contact (22) being electrically coupled to the non-top terminal (17) and the second contact (21) being electrically coupled to a terminal (16) other than the non-top terminal.

Regarding claim 12, Bates et al. discloses in e.g., Fig. 1 the plurality of contacts residing in the same plane.

Regarding claim 17, Bates et al. discloses in e.g., Fig. 1 one of the terminals (16) of the device (14) being a top contact located at the top of the device; and the package (a package in Fig. 1 without cover 13) having a package top, wherein the package top also including a contact (22) coupled electrically via (25) the conductive region to the non-top terminal (17).

Regarding claim 18, Bates et al. discloses in e.g., Fig. 1, column 5, lines 63 – 66 and column 6, lines 38 – 49 the conductive region (12, at the bottom surface of the recess) comprising a layer of metal (e.g., gold); and the electronic device (14) resides within the recess and the metal is electrically coupled to the non-top terminal (17) of the device (14).

Regarding claim 20, Bates et al. discloses in e.g., Fig. 1, column 5, lines 63 – 66 and column 6, lines 38 – 49 the metal of the conductive region (12, at the bottom surface of the recess) extending to a portion of the package top, the electronic component further comprising: a bottom contact (22) electrically coupled to the metal (12) on the package top.

Regarding claim 21, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 6, lines 38 – 49 an electronic component comprising:

- an electronic device (14) having a first terminal (16) and a second terminal (17), wherein a first dimension is defined therebetween;
- an electronic device package (a package in Fig. 1 without cover 13) having a first surface, the package formed from an integral silicon wafer (11) having a recess (at the opening or recess in the element 11) on the first surface that has a depth that is "substantially" equal to the first dimension, the package further having a layer of metal (12) applied to the recess and to a portion of the first surface, wherein the electronic device resides within the recess and is physically coupled to the package by a conductive bonding material (AuSn solder), the second terminal (17) is electrically coupled to the layer of metal (12) by the conductive bonding material (AuSn solder), and the layer of metal and the wafer are conductively coupled so as to be at "substantially" the same electrical potential (at the point or line of the element 12 and the element 11 are connected to each other has the "substantially" same electrical potential); and
- a layer of insulating (18) disposed so as to form a planar surface over the recess that is level with or higher than the top of the device.

Regarding claim 22, Bates et al. discloses in e.g., Fig. 1 a first contact (21) coupled to the first terminal (16); and a second contact (22) coupled to the metal (12) residing on the first surface of the package.

Regarding claim 32, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 6, lines 38 – 49 an electronic component comprising:

- a non-molded electronic component package (the package in Fig. 1 without cover 13) having a package top and formed from an integral silicon wafer (11) including a recess (at the opening or recess in the element 11);
- a bare die electronic device (14) having a top, a bottom, sides, and a plurality of contacts (16 and 17), the device being disposed in the recess and physically coupled to the package by a conductive bonding material (AuSn solder), wherein at least one of the plurality of contacts (17) is electrically coupled by the conductive bonding material (AuSn solder) to a metallization layer (12), the wafer and the conductive region conductively coupled so as to be at "substantially" the same electrical potential (at the point or line of the element 12 and the element 11 are connected to each other has the "substantially" same electrical potential); and
- a planarizing material (ULTEM TM polyimid siloxane resin and the element 18; column 6, line 66 – column 7, line 6) filling the recess not occupied by the device (14) and conductive bonding material (AuSn solder) to substantially create a level plane that includes the package top.

Regarding claim 35, Bates et al. discloses in e.g., Fig. 1 a second metallization layer (12) coupling one contact (22) to a redistribution point on the package top, wherein each contact remains electrically distinct (since the contact 22 is ground contact and the contact 21 is I/O's, the each contacts remains electrically distinct).

Regarding claim 36, Bates et al. discloses in e.g., Fig. 1 a plurality of conductive bumps (21 and 22), each bump being disposed at a redistribution point.

Regarding claim 40, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 6, lines 38 – 49 an electronic component comprising: the most limitations are same as claim 1 (see claim 1 rejection). However, further differences between claim 1 and claim 40 are:

- a planarizing material (ULTEM TM polyimid siloxane resin and the element 18; column 6, line 66 – column 7, line 6) filling the recess (8) not occupied by the device (1) and conductive bonding material (AuSn solder) to substantially create a level plane that includes the package top; and
- a plurality of contacts (21 and 22) including at least a first contact (22) and a second contact (21), the first contact (22) being electrically coupled to the non-top terminal (17) and the second contact (21) being electrically coupled to a terminal (16) other than the non-top terminal, wherein the plurality of contacts reside in the level plane.

Regarding claim 41, Bates et al. discloses in e.g., Fig. 1 the second conductive region (21 and the circuits that are connected the elements 16 and 21) being non-wire bonded.

Regarding claim 42, Bates et al. discloses in e.g., Fig. 1 and column 4, line 38 - 55 the layer (18) of insulation being a dielectric.

Regarding claim 43, Bates et al. discloses the conductive bumps (21 and 22) being spaced. Furthermore, the limitation "for electrically coupling with a pre-printed circuit board" is intended use language which does not differentiate the claimed apparatus over Bates et al.

Regarding claim 45, Bates et al. discloses in e.g., Fig. 1, column 4, line 38 - 55 and column 6, lines 38 – 49 an electronic component comprising:

- a silicon wafer (11) having a recess (at the opening or recess in the element 11);
- a bare die electronic device (14) having first (17) and second (16) contacts, the device being disposed in the recess and physically coupled to the wafer by a conductive bonding material (AuSn solder), the first contact (17) electrically coupled by the conductive bonding material (AuSn solder) to an electrically conductive region (12),
- the electrically conductive region (12) electrically coupling the first contact (17) and the wafer to an electrical input (22; an electrical input to the electronic component from the die) of the electronic component, wherein the second contact (16) is electrically coupled by non-wire bonding to a second electrical input (21) of the electronic component, and
- a dielectric material (18) disposed so as to form a planar surface over the recess that is level with or higher than the top of the device.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 13, 15, 44, 47 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al. in view of Mahulikar et al. '835.

Regarding claim 13, Bates et al. does not disclose a second layer of dielectric completely covering the silicon wafer and the device except for the plurality of contacts. However,

Mahulikar et al. teaches in e.g., Fig. 7 a second layer of dielectric (26) completely covering a substrate (52) and a device (54) except for the plurality of contacts (44). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bates et al. by using the second layer of dielectric to completely cover the silicon wafer and the device except for the plurality of contacts as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Bates et al. in the manner described above for at least the purpose of protecting the die and the wafer.

Regarding claim 15, Bates et al. does not disclose the second conductive region being a solder bump. However, Mahulikar et al. teaches in e.g., Fig. 12 a solder bumps (solder balls or 70) in a second conductive region (an area under the solder balls). Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bates et al. by using the solder bumps as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Bates et al. in the manner described above for at least the purpose of increasing the bond strength between the package and the external device (e.g., PCB).

Regarding claims 44 and 47, Bates et al. discloses in e.g., Fig. 1 and column 4, line 38 - 55 the bare die electronic device (14) being covered by the dielectric material (18). However, Bates et al. does not disclose the electronic component being a flip chip. Mahulikar et al. teaches in e.g., Fig. 17 an electronic component (170) being a flip chip. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bates et al. by using the electronic component to be a flip chip as taught by Mahulikar et al. The ordinary artisan would have been motivated to modify Bates et al. in the manner described above

for at least the purpose of providing an ease manufacture and reliability (column 10, lines 13 - 16).

Regarding claim 48, Bates et al. discloses in e.g., Fig. 1 and column 4, line 38 - 55 the silicon wafer (11) being an integral piece of silicon.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bates et al. in view of Yoshida et al. (JP 59-145537) or Oji et al. (JP 58-197857)

Bates et al. discloses the claimed invention except the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. However, Yoshida et al. or Oji et al. discloses the conductive region comprises: a first layer of titanium; a second layer of copper deposited on the first layer; and a third layer of chrome deposited on the second layer. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Bates et al. by adding the conductive region as taught by Yoshida et al. or Oji et al. The ordinary artisan would have been motivated to modify Bates et al. in the manner described above for at least the purpose of increasing adhesive strength between the conductive region and the device.

Response to Arguments

7. Applicant's arguments with respect to claims 1, 14, 16, 21, 32, 40 and 45 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is (703) 305-6194. The examiner can normally be reached on M-F (10:30 - 7:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone number for the organization where this application or proceeding is assigned is (703) 308-7382.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Chris C. Chu
Examiner
Art Unit 2815

c.c.
Thursday, July 08, 2004

Tom Thomas

TOM THOMAS
SUPERVISO[illegible] MINER
TECHN[illegible] 2800